Mechanically Operated Random Access Memory (MORAM) Based on an Electrostatic Microswitch for Nonvolatile Memory Applications

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***Abstract*—We proposed and demonstrated a mechanically operated random access memory (MORAM) based on an electrostatically actuated metallic microswitch for nonvolatile memory applications. The metallic microswitch-based MORAM successfully showed program and erase operations, wherein the microswitch had an essentially zero off current, an abrupt switching with less than 1 mV/dec, and an on/off current ratio over 10^7, and its stored charge was investigated with the metal–oxide–semiconductor (MOS) capacitor. Moreover, first reported were an endurance of up to 10^5 cycles in air ambient and a retention time of more than 10^4 s in vacuum ambient.**

***Index Terms*—Abrupt switching, dynamic random access memory (DRAM), electrostatic microswitch, endurance, microelectromechanical systems (MEMS), nonvolatile memory, retention.**

I. Introduction

OVER the past four decades, there has been a tremendous advancement in the semiconductor industry, thanks to the aggressive scaling of MOSFETs. However, many difficult challenges in continuing to scale down beyond sub-100 nm have been encountered so far, such as power dissipation, parasitic leakage current, and short-channel effects [1], [2]. In recent years, novel microelectromechanical systems (MEMS) [3]–[5] and nanoelectromechanical systems (NEMS) [6]–[9] devices have emerged as one of the promising solutions, considering that they have excellent on/off characteristics due to an essentially zero off current and an abrupt switching.

MEMS/NEMS devices have already had a noteworthy impact on various areas, such as in radio-frequency circuits, automotive, and aerospace [10], and are being expanded to enable revolutionary advances for future memory applications [11]–[21]. However, existing memory devices using MEMS/NEMS technology are still far from realization due to numerous hurdles such as fabrication difficulty, stiction, high operation voltage, and device scalability. Recently, we reported a new memory-cell structure based on a poly-Si microswitch for nonvolatile memory applications [5].

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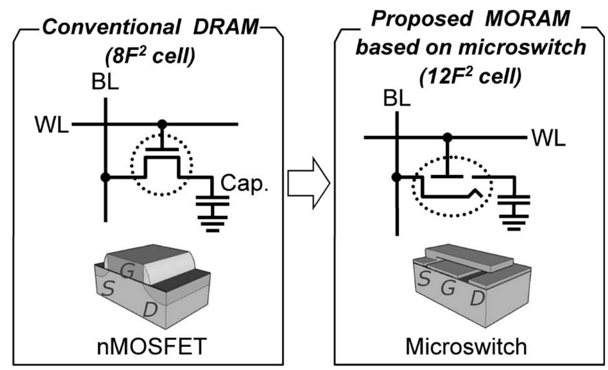


Fig. 1. Schematic diagram and equivalent circuit of the conventional DRAM and the proposed MORAM based on the microswitch, which is similar to the DRAM except that the nMOSFET is replaced with the metallic microswitch.

In this brief, we consolidated the concept of the microswitch-based mechanically operated random access memory (MORAM) by replacing the poly-Si microswitch with a metallic microswitch. The metallic microswitch with a gold-to-gold (Au-to-Au) contact eliminates the native oxide-related contact problems of our previous works and then reliably avoids the stiction-related device failures. Moreover, the endurance and retention properties of the fabricated MORAM were first investigated.

II. Device Structure and Fabrication

The microswitch-based MORAM is simply composed of one electrostatic microswitch and one storage capacitor, where the memory-cell structure is quite similar to that of a conventional dynamic random access memory (DRAM), as shown in Fig. 1. In contrast to DRAM, which loses data due to the inevitable leakage current of the MOSFET when the supply power is cut off, the proposed memory has "nonvolatile" memory characteristics because the microswitch can completely eliminate the off-state leakage current due to the physical isolation between the source and the drain or between the source and the gate; thus, the charge leakage path from the storage capacitor through the off-state microswitch does not exist. For the cell design, the MORAM is expected to have areas of 12 F^2, which are larger than that of a common DRAM structure (8 F^2); however, the effective cell size can be dramatically decreased by wafer-level 3-D stacking technology.

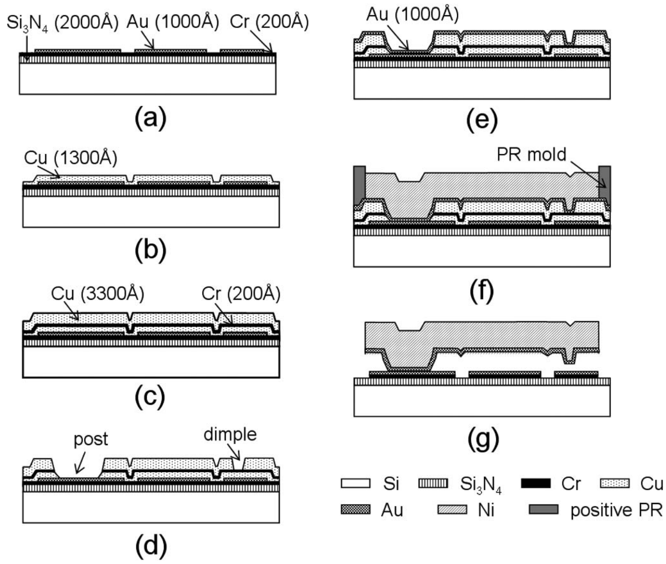


Fig. 2. Simplified fabrication process of the metallic microswitch-based MORAM using a metal surface micromachining technology. (a) Bottom electrode formation. (b) Cu sacrificial deposition. (c) Cr/Cu sacrificial deposition. (d) Dimple and post wet etching. (e) Au deposition for contact. (f) Ni beam plating (1.7 μm). (g) Sacrificial etching and Ni beam release by CPD.

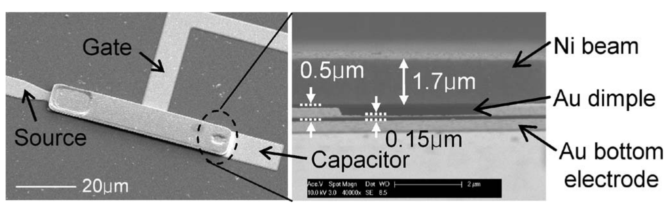


Fig. 3. SEM images of the fabricated microswitch-based MORAM and a magnified view of the air-gap region between the suspended Ni beam and the Au bottom electrode.

Fig. 2 shows the simplified fabrication process of the metallic microswitch utilizing a metal sacrificial layer [22]. In particular, we chose thick electroplated nickel (Ni) with high Young's modulus of 200 GPa as the structural material of the suspended beam and the Au-to-Au contact with good resistance to oxidation to obtain a highly reliable microswitch. Double sacrificial layers of Cu were deposited by thermal evaporation in order to precisely control the thickness of the air gap. After fabricating the suspended Ni beam, those two Cu sacrificial layers were selectively etched by acetic acid etchant, leaving all other materials unaffected, and a critical point drying was finally conducted to prevent stiction between the Au dimple and the Au bottom electrode.

Fig. 3 shows the scanning electron microscope (SEM) images of the fabricated MORAM cell and a magnified view of the aforementioned air gap. The straight suspended Ni beam is formed without any deformation, and the Cu sacrificial was well removed without leaving any residues in the air gap.

III. Results and Discussion

Fig. 4(a) shows the electrical characteristics of the fabricated metallic microswitch. A minimum voltage, so called the pull-in voltage, to turn on the microswitch with 40 μm in length, 8 μm in width, and 1.7 μm in thickness was about 22 V. The electric current can flow between the source and the drain when applying a gate voltage $(V_{G,\,\mathrm{switch}})$ which is slightly larger than the pull-in voltage of the microswitch. Here, a compliance current of 10 μA was used to prevent in-use stiction between the Au dimple and the Au bottom electrode mainly caused by Joule heating due to the high current density. The fabricated microswitch showed ideal on/off current characteristics with an essentially zero off current, an abrupt switching with less than 1 mV/dec (practically infinite), and a high on/off current ratio exceeding 10^7, which were limited to the measurement conditions such as the voltage step and the compliance current. As shown in the inset of Fig. 4(a), the fabricated microswitch had a typical hysteresis curve with the pull-in and pull-out phenomena common with conventional MEMS switches. These switching characteristics of the fabricated microswitch are the most important factors for achieving the nonvolatile memory characteristics of the proposed MORAM. Moreover, the switching speed of the MORAM is determined and limited by the natural resonant frequency of the suspended Ni beam in the metallic microswitch, which can be easily estimated using the equation given by $f = (1.02/2\pi)(t/L^2)\sqrt{E/\rho}$, where E is the Young's modulus, ρ is the density, t is the thickness, and L is the length [10]. The minimum switching time of the MORAM is approximately calculated as 1.2 μs for $L = 40$ μm, $t = 1.7$ μm, $E = 200$ GPa, and $\rho = 8908$ kg/m^3, corresponding to the switching frequency of 0.8 MHz.

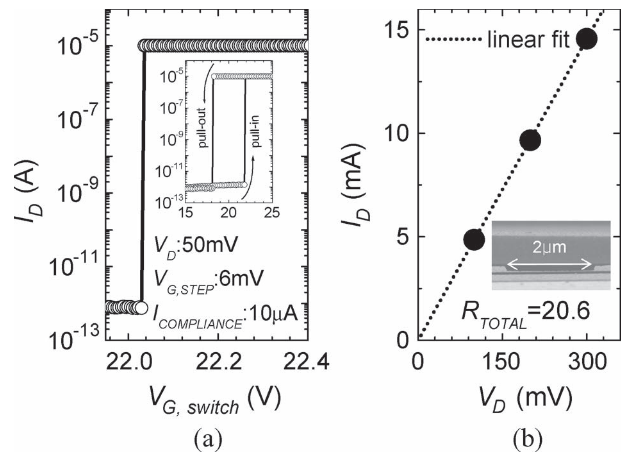
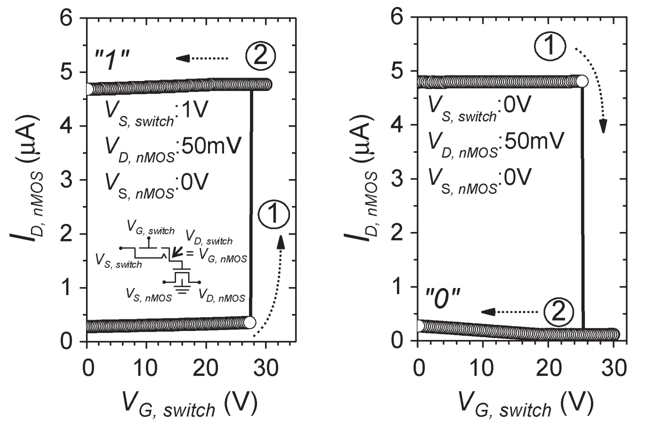


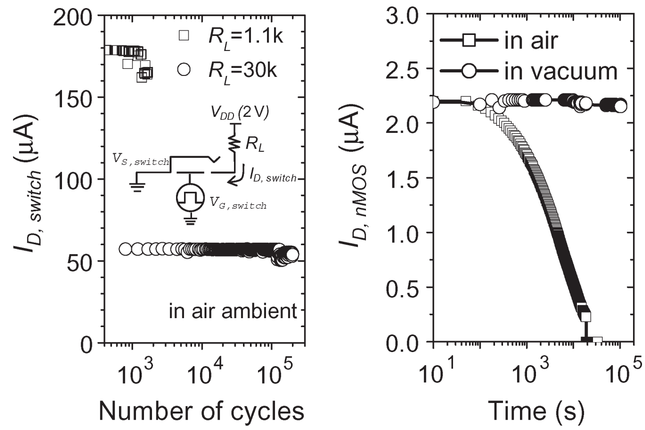
Fig. 4. (a) I_D versus $V_{G,\,\mathrm{switch}}$ characteristics. (b) I_D versus V_D characteristics showing the total on resistance of the fabricated microswitch.

Fig. 4(b) shows the drain current (I_D) versus the drain voltage (V_D) characteristics of the fabricated metallic microswitch. The maximum on current was measured to be 15 mA at the drain voltage of 300 mV. A total on resistance of the microswitch, including probe tips, is approximately 20 Ω, which is relatively larger than that of other MEMS switches, because the fabricated microswitch had a small contact area between the Au bottom electrode and the Au dimple which has a radius of 2 μm, as shown in the inset of Fig. 4(b). However, the contact-resistance-related problems of the microswitch are expected to



(a) (b)

Fig. 5. $I_{D,\mathrm{nMOS}}$ versus $V_{G,\mathrm{switch}}$ for showing the (a) program operation and (b) erase operation of the fabricated MORAM, where the number in the circle shows the sweep sequence of the $V_{G,\mathrm{switch}}$. The inset shows the experimental setup for characterizing memory operations of the fabricated MORAM.



(a) (b)

Fig. 6. (a) Endurance and (b) retention characteristics of the fabricated microswitch-based MORAM.

be solved by employing various techniques such as increasing the contact area using multiple dimples or an enlarged tip of the suspended beam.

The experimental setup for investigating the memory operations of the fabricated MORAM is shown in the inset of Fig. 5(a). Instead of the metal–insulator–metal capacitor, we used the MOS capacitor of the nMOSFET as a simple and effective apparatus to demonstrate the memory operations, endurance, and retention characteristics of the fabricated MORAM without any additional sensing circuitry. Here, the individual microswitch and the nMOSFET were electrically connected by wire bonding. Note that the long-channel nMOSFET, with a gate oxide thickness of 35 nm, a gate length of 10 μm, and a gate width of 50 μm, was used and the threshold voltage of the MOSFET was 0.3 V.

Fig. 5(a) and (b) shows the drain current of the nMOSFET $(I_{D,\mathrm{nMOS}})$ versus the gate voltage of the microswitch $(V_{G,\mathrm{switch}})$ for showing the memory operations of the fabricated MORAM. They describe the program operation for charging the MOS capacitor and the erase operation for discharging the MOS capacitor such as DRAM. As soon as the microswitch is electrostatically turned on by applying a voltage larger than the pull-in voltage to the gate, the source voltage of the microswitch (in this case, $V_{S,\mathrm{switch}} = 1$ V) is transferred to the drain of the microswitch and to the gate of the nMOSFET at the same time. The nMOSFET is then turned on; the electric current flows between the source and the drain of the nMOSFET, and the memory cell is eventually programmed. As shown in Fig. 5(a), the $I_{D,\mathrm{nMOS}}$ value maintains the "one" state even when the $V_{G,\mathrm{switch}}$ is turned off because the gate of the nMOSFET becomes a floating gate. On the contrary, the memory cell is erased when the microswitch conveys 0 V to the gate of the nMOSFET. When the microswitch is turned on once again, the source voltage of the microswitch (in this case, $V_{S,\mathrm{switch}} = 0$ V) is transferred to the drain of the microswitch and then to the gate of the nMOSFET. The nMOSFET is then turned off, and the electric current does not flow any longer between the source and the drain of the nMOSFET, as shown in Fig. 5(b). Now, the $I_{D,\mathrm{nMOS}}$ value changes from the "one" to the "zero" state and then stays in the "zero" state when the microswitch is off. This way, the program and erase operations of the proposed microswitch-based MORAM was successfully verified.

Fig. 6(a) shows the endurance property of the fabricated microswitch. In hot switching conditions, the drain current of the microswitch $(I_{D,\mathrm{switch}})$ was measured in air ambient as a function of switching cycles having the drain connected to V_{DD} of 2 V through two different load resistors to see how the current density affects the endurance. Here, an ac bias, with a peak voltage of 25 V and a square wave of 100 Hz, was applied to the $V_{G,\mathrm{switch}}$, and a zero voltage was applied to the $V_{S,\mathrm{switch}}$. As shown in Fig. 6(a), we observed that the large load resistance (small current density) drastically improved the endurance of the microswitch. The $I_{D,\mathrm{switch}}$ values started to deteriorate after about 10^5 cycles. The Au–Au contact properties are thought to be degraded as the contact surface of the drain is physically damaged and eventually welded after certain cycles by repeated operations in air ambient. However, the endurance appears to be greatly improved when measured in a vacuum and N_2 ambient. Consequently, the microswitch will have a higher endurance by introducing the gold-alloy contact [23] and hermetic sealing [24]. Fig. 6(b) shows the retention property of the fabricated metallic microswitch-based MORAM. After the memory cell was programmed, the drain current of the nMOSFET $(I_{D,\mathrm{nMOS}})$ versus time was monitored both in air and vacuum ambients. The $I_{D,\mathrm{nMOS}}$ value in air ambient slowly decreased as time elapsed. On the other hand, the $I_{D,\mathrm{nMOS}}$ value remained almost unchanged until 10^4 s in vacuum ambient. We think that the dominant mechanism of charge leakage is caused by the leakage of the charge stored in the MOS capacitor due to water vapor in the atmosphere [25] including the gate leakage of the nMOSFET. These results show that if properly packaged, the fabricated MORAM is expected to show feasibility as a new memory device with good endurance and retention properties that are attractive for use in future nonvolatile memory applications.

IV. CONCLUSION

We developed a metallic microswitch-based MORAM by replacing the switching transistor of the conventional DRAM with a metallic microswitch, which eliminates any leakage current owing to the physical isolation by the air gap. The fabricated MORAM showed good endurance and retention properties using the Au-to-Au contact microswitch with ideal on/off current characteristics and an essentially zero off current, an abrupt switching with less than 1 mV/dec, and an on/off current ratio exceeding 10^7. We still have many challenges, such as the difficulty of downsizing the microswitch to a nanoswitch, a high contact resistance, and low endurance; however, this kind of mechanical-type memory device is thought to be worth pursuing due to its excellent memory characteristics, as demonstrated in this brief.

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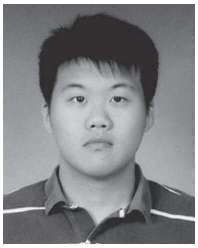

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